Design an Energy Efficient Carry Speculative Adder
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Abstract:
We proposed an Adder called Carry Speculative Adder with low power consumption and reduced delay. The structure is based on partitioning adder into some non overlapped summation blocks whose structure may be selected from parallel-prefix and carry propagate adders. Based on input operands the carry output of each block is speculated. We choose BKA because it is one of the parallel-prefix adder. To reduce delay BKA is used to perform logical operations. It consume maximum depth and less area. In this adder the length of the carry chain is reduced to two blocks. From this block we can calculate the lower average delay. To improve the accuracy and to tolerate error, error detection and recovery mechanism is used. Carry Speculative Adder posses low delay, area and better output quality. Comparing other parallel prefix adder CSA including BKA is more efficient.


I. INTRODUCTION
The power consumption reduction and speed improvement are the key goals in the design of digital circuit is general. One of the approach to improve both the power and speed is to approximate adders. Approximate adders have been received many attention by the designers. Adder blocks, which are the main components in arithmetic units of DSP systems, are power hungry and often from hotspots locations on the die. Prior researches on approximate adders have taken two general approaches of focusing on error weight and error probability reduction. For these adders, reducing the error probability of the summation as well as reducing the power and delay are the key design criteria. They may also accompanied by an error correction unit which has time, power and area overheads. Approximate arithmetic units are mainly based on the simplification of the arithmetic units circuits. Different structures for approximate adders are fully approximate and only be utilized in error re silent applications. Here ,by reducing the quality, the total computation time and/or power consumption of the unit are reduced resulting in higher energy degradation. The main reason behind this is that in binary arithmetic, adders are the main component to perform mathematical operations. Besides arithmetic operations, adders are used to perform increment, decrement, and many similar operations. Therefore, being the most widely used fundamental data operators, adders have attracted a noteworthy attention for approximation. Since delay and power of adders increase rapidly with bit-width (N), for a marginal improvement in delay/power, we have to sacrifice an immense amount of power/energy. Consequently, at a micro architecture level of abstraction, adders have become the key delay/power bottleneck of digital systems. One possible way to overcome this situation is to approximate adders, that is, to sacrifice accuracy for delay and/or power. In some applications such as image processing or audio/video compression, the required accuracy might vary during run time. To meet the need for runtime accuracy adjustment, a series of designs are developed to implement accuracy-configurable approximation, which could be reconfigured online to save more power.

A new carry-prediction based accuracy configurable adder design:
Simple accuracy configurable adder (SACA). It is a simple design with considerably less area than CLA, which, to the best of our knowledge, has not been achieved in the past in ACAs. SACA inherits the advantages of all previous carry-prediction-based approaches: no error correction overhead, no data stall, and allowing graceful degradation.

II. RELATED WORKS
To design of low power 16-bit novel carry select adder using 0.18um technology MLavanya D, department of ECE Vardhaman college of Engg. Nageshwar Rao Department of ECE TKR College of Engg. And Tech K.Rama Krishna Department of ECE TKR College of Engg. And tech An appropriate approach is proposed in this paper to reduce the area and power of 16-bit novel CSLA. The reduced number of gates of this work provides reduction of space and energy consumption. The comparison results show that the area and power of 16-bit novel CSLA are significantly reduced by 62% and 27%respectively. The 16-bit novel CSLA architecture by sharing common Boolean logic term is therefore, low area, low power, simple and efficient for VLSI hardware implementation. Speculation adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders. In speculative adders sum and carry part is separated to reduce the area overhead. Carry speculative adder(CSPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to find the fault occurred in the partial sum generator and to recover it to get accurate results. This speculative adder can reduce the delay upto 11.88%.
A reviews classifications and comparative evaluations of Approximate arithmetic circuit HONGLAN JIANG,
University of Alberta cong liu, tsinghua university
FABRIZIO LOMBARDI, northeastern university
JIE HAN, university of Alberta.

Often as the most important arithmetic modules in a processor, adders, multipliers and dividers determine the performance and the energy efficiency of many computing task. The demand of higher speed and power efficiency, as well as feature of error resilience in many applications (e.g. multimedia, recognition and data analytics), have driven the development of approximate arithmetic design. A comprehensive and comparative evaluation of their error and circuit characteristics is performed for understanding the features of various designs. This circuit used in image processing applications consumes as little as 47% of the power and 36% of power-delay product of an accurate design while achieving a similar image processing quality. Improvement in delay, power and area are obtained for the detection of differences in image by using approximate dividers.

III. PROPOSED SYSTEM:

In electronics, addition of the binary numbers in various computers and other types of processors are performed by the adders. Adder circuits are used in various processors for calculating increment or decrement operations, table indices, addresses etc.

A. SPECULATIVE CARRY SELECT ADDER:

Carry chain in the addition process is observed for the design of speculative carry select addition(SCSA). The carry chain is observed because the long carry chain is rarely activated in the block adders. To overcome this problem, in SCSA the input bits are divided into two parts of equal sizes. A group of consecutive input bits are given as input to a single block adder. A block adder is known as the window, the number of consecutive input bits is known as window size and it is denoted by K. number of windows to be used is found by M=N/K where, n is the total number of input bits. 

B. SPECULATIVE ADDITION:

Speculative addition is widely used in asynchronous design. The speculative addition involves two cycles. In the first cycle, the addition process is done and the end result is assumed as accurate sum. Meanwhile, a parallel carry propagation circuit checks whether the operation uses the carry long path known as the critical path. If it uses the longest path the system requires the additional clock cycle to complete the addition process. If it didn’t use the longest path, bypass logic is used to reduce the clock cycle required. decimal(BCD) and gray code can be added using the adder circuits. Adder found wide range of applications in many fields and for many operations such as decoding, calculation etc. The critical path is not often activated in traditional adders, based on this observation speculative adders have been designed. Traditional adders depend on its precious values for its each output. Particularly, the MSB of the sum depends on all the n bit previous outputs, where n is the block adder width. As the width of block adder increases, there will be an error growth. The error grows linearly with n. there will be a large area and large fan out at the primary inputs due to this error. Speculative adders can overcome the area problem but it has high error rate. For this error tolerant variable latency adder is design upon the speculative adder. This variable latency adder consists of error recognition and correction circuit, which can overcome the high error rate and this design helps the speculative adder to use in many applications such as image and signal processing Consider

C. BRENT KUNG ADDER

It is one of the arithmetic adder. It occupies very little space. It has maximum depth. It posses less gates inside. It is more efficient in terms of speed and power.

D. SYSTEM MODEL

![Figure 1. System model of carry speculative adder](http://ijesc.org/)

The different formats like XS-3, binary coded faster but the possibility of occurrence of error is increased. The proposed speculative adder can be able to complete the addition process quickly when compared to the existing technique speculative sum bit is calculated by the carry out bit of the window. By this prediction technique, the addition

Consider two inputs A and B, A=01, B=10.

**First cycle:** Addition is done without carry Second cycle: addition is done with Carry Speculative adder. It contains brent-kung adder for performing both cycles. Enable and clock signals are used to enable inputs. Error detection unit is used to detect error in the inputs. Error recovery unit is there to perform ex-or operation to recover input from error. Two inputs are given to multiplexer. Based on selection line accurate output appears. Brent-kung adder is selected from block of adder. The reason behind using BKA, it provides less delay comparing other types of adders. There may be a trade off between delay and other parameter such as area, power, output accuracy etc., carry Select adder is widely used to improve performance of adders accuracy without increase.
E. ERROR RECOVERY AND ANALYSIS

There are two possible cases of errors. The major advantage
\[ C_i^{\text{out}} = G_i^{\text{x-1:i-0}} + P_i^{\text{x-1:i-0}} C_i^{\text{out}} - 1 \]
The different formats like XS-3, binary coded faster but the possibility of occurrence of error is increased. The proposed speculative adder can be able to complete the addition process quickly when compared to the existing technique speculative sum bit is calculated by the carry out bit of the window. By this prediction technique, the addition is that the error detection unit can find which block adder prediction is wrong. By this advantage the work of the recovery circuit is simplified. The recovery circuit rectifies the affected block adder and corrects the output so that the output sum is accurate. This circuit is designed using varying latency design so that if an addition process is completed it send a valid signal to the input side to fetch another set of inputs to perform addition. A variable latency adder that combines the speculative adder with error recognition and correction for unsigned random inputs, called variable latency CSPA. The sum and carry generation are separated in CSPA and thus the carry signal and partial sum bit can be calculated faster. Carry predictor circuit of the block adder only to use input bits near the MSB to predict the carryout bit. The hardware cost of the prediction circuit is reduced and the CSPA has minimal error rate increase. The proposed error detection circuit indicates which block adder produced in incorrect carry-out bit, and the error recovery circuit only focuses on recovering the block adders with incorrect partial sum bits. On comparing CSPA and SCSA, CSPA reduces 11.88% delay and also reduces computational complexity upto 11.38%.

There are two possible cases of errors. Case (i)pix /x-x-k/= I and Gi x-k:/O = I, Case (ii)P-x-1:/O= I and Gi -I x-x-k= I,

IV. SIMULATION RESULT

4.1. SOFTWARE TOOL DESCRIPTION:
Xilinx ISE (Integrated Synthesis Environment) is a software tool. It will be helpful for simulation as well as implementation. We can synthesis power distribution, delay, no of LUTs used, flooring plan and simulation results.

4.2. SIMULATION RESULTS:

(i) BCSA without ERU (8 bit) using RCA

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<th>0.5</th>
<th>1.0</th>
<th>1.5</th>
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Figure 2. Simulation Result of BCSA without ERU (8 bit) using RCA

(ii) BCSA_ERU-(8 bit) using RCA

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<th>1.0</th>
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Figure 3. Design Summary of BCSA without ERU (8 bit) using RCA

Figure 4. Timing Summary of BCSA without ERU (8 bit) using RCA

Figure 5. Power Analysis of BCSA without ERU (8 bit) using RCA

Figure 6. Simulation Result of BCSA_ERU-(8 bit) using RCA
Figure 7. Design Summary of BCSA_ERU_(8 bit) using RCA

Figure 8. Timing Summary of BCSA_ERU_(8 bit) using RCA

Figure 9. Power Analysis of BCSA_ERU

(iii) ECSA without ERU 16 bit

Figure 10. Simulation Result of ECSA without ERU 16 bit

Figure 11. Design summary of ECSA without ERU 16 bit

Figure 12. Timing Summary of ECSA without ERU 16 bit

Figure 13. Power Analysis of ECSA without ERU 16 bit

(iv) BCSA with ERU (16 bit)

Figure 14. Simulation Result of BCSA with ERU (16 bit)
(vi) 16 BIT APPROXIMATE ADDER COMPARISON TABLE:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>BCSA without ERU using RCA</th>
<th>BCSA with ERU using RCA</th>
<th>BCSA with ERU using Brent Kung adder</th>
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</thead>
<tbody>
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<td>23</td>
<td>21</td>
</tr>
<tr>
<td>Number of 4input LUTs</td>
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<td>33</td>
<td>32</td>
</tr>
<tr>
<td>Delay (ns)</td>
<td>13.97</td>
<td>13.372</td>
<td>13.051</td>
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<tr>
<td>Power (W)</td>
<td>0.172</td>
<td>0.172</td>
<td>0.172</td>
</tr>
</tbody>
</table>

V. CONCLUSION AND FUTURE WORK

In this paper, we proposed a adder called as energy efficient carry speculative adder CSPA, which was based on dividing an exact adder into some non-overlapped blocks operated in parallel. Each block may be composed of any desired type of adders. In this we used carry select adder. It contains two ripple carry adders and one multiplexer. It performs addition with carry and without carry and generates accurate sum based on selection line of the multiplexer. Error detection and recovery unit is present to overcome all error occurring problem. A select logic
was suggested to speculate the carry input of each block based on some input operand bits of the current and next block. In addition, to decrease the accuracy loss, an error detection and recovery mechanism was suggested. Based on the results, for the different approximate operating modes. It decreases the delay and improves performance and output accuracy.

VI. REFERENCES


VII. AUTHORS

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