Performance Analysis of Low Power High Speed Hybrid Full Adder
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Abstract:
In this paper, we have designed an ALU in a reversible logic using reversible gates like Feynman gate, Fredkin gate etc. The hybrid full adder was designed by using the weak inverter (by using the transistor) and strong transmission gate using Cadence Virtuoso tool in 180-nm technology. The weak inverter was used to design the XNOR gate and the transmission gate was used to design a carry module. The weak inverter used to reduce the power consumption by reducing the voltage degradation. The parameters such as power consumption, propagation delay were calculated for the adder. For 1.8-V supply at 180-nm technology, the average power consumption (13.89 mW) was found to be extremely low with moderately low delay (111.2ps) resulting from the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. This ALU consists of ten operations, 2 arithmetic, 4 logical operations and 4 shifting operations. The ALU performs better than the normal ALU.

Keywords: ALU, Adder, Propagation delay, Power consumption

I.INTRODUCTION

The adders are used in many applications such as calculators, mobile phones, computers, laptops, digital calculators. As the technology gets improves by year, the size of these devices get reduced. Hence the circuits inside it should be reduced. The adders with minimum use of transistors and delay have to be used. Standard static complementary metal–oxide–semiconductor (CMOS) [3], dynamic CMOS logic complementary pass-transistor logic (CPL) and transmission gate full adder (TGA) [7], [8] are the most important logic design styles in the conventional domain. ALUs, being one of the most fundamental building block of all the applications. Intoday’s technology it plays an important role. Hence, the design of low power consumption and low power delay ALU circuit is important for all circuits. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of bits. Hence the Reversible circuits were introduced. The circuits were designed using the reversible gates. The reversible circuit connect reversible gates without loops and fan outs. Hence this circuit have equal number of inputs and outputs. Hence there is a one to one mapping between the input and output vectors. Hence the number of bits used is reduced.

II.DEIGN OF HYBRID ADDER

The hybrid adder in this paper is designed using XNOR circuit. The transmission gate logic and weak inverter is used to design the XNOR circuit. XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1land Mn1. The output of the carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8. The input carry signal (Cin) propagates only through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path. The circuit of full adder is given below

Figure 1. Circuit of full adder

III.DEIGN OF ALU

Arithmetic and Logic Unit (ALU) is one of the most power consuming components in a microprocessor. So, to reduce the power consumption of the entire ALU each of its components should consume less power. Hence the reversible logic is used to reduce the power consumption of the circuit. The ALU contain arithmetic, logical and shifting operations. The proposed full adder is used in the arithmetic block of the ALU. Hence the power consumption and propagation delay of the arithmetic block is further reduced.

3.1 ALU block diagram

Figure 2. ALU circuit
The arithmetic unit consists of half adder, fulladder, half subtractor and full subtractor. In logic unit, AND, OR, NOT and XOR gates are present and additionally there is shifters and multiplier units.

3.2 ALU operations

Table.1. operations of ALU

<table>
<thead>
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<th>S1</th>
<th>S0</th>
<th>Operation performed</th>
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<td>0</td>
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<td>1</td>
<td>X</td>
<td>X</td>
<td>multiplier</td>
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IV. RESULT FOR FULL ADDER

The power consumption in 1 bit full adder is at the range of 13.89 mW. If we use buffer, there is reduction in power. Propagation delay in the full adder circuit is about 111.2 ps. The figure below shows the simulation result of the full adder.

![Simulation result of Full adder](image)

V. RESULT OF ALU

The delay of the proposed ALU is 14.02ns while the delay of the normal circuit is 19.09ns.hence the delay is reduced by using reversible gates and the hybrid full adder circuit.

VI. CONCLUSION

Hence the ALU designed using the hybrid full adder gives minimum propagation delay. The full adder consumed only less amount of power. Hence the power consumption of the various devices can be reduced by using this full adder circuit In future this ALU can be used in various devices. Here we have designed 4-bit ALU circuit we can also design 8 bit, 16 bit ALU circuits by using reversible logic.

VII. REFERENCES

[1]. Partha Bhattacharyya, Senior Member, IEEE, Bijoy Kundu, Sovan Ghosh, Vinay Kumar, Member, IEEE, and Anup Dandapat, Member, IEEE, vol. 23, no. 10, October 2015


