Design of Low-Power Capacitor Free Low-Dropout Regulator

G Ahmed Zeeshan1, Dr. R Sundara Guru2, G Laxmi3
Assistant Professor1, Ph.D., Professor and Head2, M.Tech3
Department of Electronics and Communication Engineering
Global Institute of Engineering and Technology, Moinabad, Hyderabad, Telangana, India1,3
MVIT, Bangalore, Karnataka, India2

Abstract:
A low-voltage Low-DropOut (LDO) regulator that converts an input of 1.8 V to an output of 1.7 to 1.8 V, with 90-nm CMOS technology is proposed. A simple symmetric operational transconductance amplifier is used as the Error Amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. This result performs on the H-spice tool at 90 nm.

Index Terms: Fast transient response, high power supply rejection, Low-DropOut (LDO) regulator, low-voltage, small area.

I. INTRODUCTION
Power management unit with several integrated regulators is widely used in modern battery-powered portable devices. These power management schemes often use a primary switching regulator and several post regulators. The primary switching regulator converts the high DC voltage level of the battery (e.g., 4.2–2.7 V) into a low DC voltage level (e.g., 1 V) with a high conversion efficiency (>90%). The post regulators also generate several independent power sources for multiple voltage domains. The switching regulator inevitably generates voltage ripples over the range of the switching frequency. The switching frequency of the regulator often lies within a low-frequency band of a few 10–100 kHz to reduce switching power loss. The post-regulators should, therefore, be able to provide a good Power Supply Rejection (PSR) ability to suppress these unwanted low-frequency noises. To further maintain high power efficiency, minimize the impact on target load circuits, and reduce cost, the post regulators must operate at low voltage and low quiescent current (IQ), achieve a fast transient response with a small output variation, and minimize their area. The Low-DropOut (LDO) regulator has a simple architecture and a fast-responding loop, which makes it the best candidate to implement these post-regulators. A number of previous papers focused on enhancing the transient response or the PSR or both of LDO regulators. The designs use either a large driving current or additional circuits, which consume a significant IQ. The design consumes a small IQ, yet has a large output variation during the load transient. The dynamic biasing technique is widely adopted by conducting a very small IQ under a light load condition. This inevitably sacrifices the transient response during a light to heavy load current transition. The LDO Regulators proposed and achieved a high PSR over a very wide frequency range (up to 10 MHz). Using bipolar junction transistor process technology or a complex ripple cancellation circuit to achieve a PSR > 10 MHz at the expense of a high IQ is, however, unnecessary for the post regulator of a general purpose switching regulator. Further, a complex compensation circuit or a high-gain cascade Error Amplifier (EA) complicates the LDO regulator design and is not feasible for low-voltage systems (≤1 V) that are using advanced technology. All the previous regulators are unable to achieve sub 1.8-V operation.

II. DESIGN CHALLENGES AND CONCEPTS OF THE PROPOSED LOW-VOLTAGE LDO REGULATOR
A basic LDO regulator is mainly composed of a biasing circuit, an EA, a power MOS transistor (MP), and a feedback network, as shown in Fig. 1. Now, the Transient Accelerator (TA) is removed. An off-chip output capacitor (CL) is used to mitigate the output variations during the load transient. The design challenges and concepts in designing a low voltage LDO regulator are summarized briefly in the following sections.

A. Low Supply (Input) Voltage and Low IQ
A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable IQ that are proposed to enhance performance. A MP with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA requires a higher current slew rate to drive the MP. To achieve low-voltage operation, an EA with not more than three stacked transistors between the supply voltage and ground is preferred; each of the transistors, therefore, has more voltage space to stay in the saturation region. A possible candidate can be as simple as an Operational Transconductance Amplifier (OTA) with a low-cost gain-boosting technique like current splitting. The EA also requires a wide output swing to minimize the size of the M, and hence relieve the requirement on output current slew rate of the EA.

B. Fast Transient Response
The transient response includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation (e.g., 50 mV) can cause severe performance degradation to the load circuit
operating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required. Increasing the closed-loop bandwidth may, however, affect the pole/zero locations and the circuitry may become too complex, consuming more IQ. The concept of the TA, shown in Fig. 1, is, therefore, adopted to conditionally provide extra charging/discharging current paths (slew current), depending on the status of the output variation detector.

C. Power Supply Rejection
To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An n-type power MOS transistor or a cascaded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a p-type power MOS transistor, either a high loop gain or good noise cancellation at node VG can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra IQ [2]. The concept of resources sharing power noise cancellation mechanism as shown in Fig. 1 is thus proposed. The first stage (stage 1_EATA) of the EA attenuates the power noise, whereas the second stage (stage 2_EA) of the EA rejects the common mode noise (\(v_{\text{icm}}\)) at its inputs, and creates a replica of the supply noise at the output. The stage 1_EATA is shared by the EA and TA, saving the cost and IQ.

D. Small Area
In a low-voltage LDO regulator design, several performance enhancing auxiliary circuits and a large MP occupy considerable space. A wide output swing EA can reduce the size of the MP. To support a wide load current range (e.g., 0–100 mA) and a wide output-voltage range (e.g., 0.5–0.85 V), the MP may enter the triode region when under a heavy load condition (large \(V_{\text{SG}}\)) with a low-dropout voltage (small \(V_{\text{SD}}\)). The MP should, therefore, be large enough to make the intrinsic gain of the MP close to one at the triode region and maintain a high loop gain in the LDO regulator. Similarly, the LDO regulator can respond to the load current transient in time for such a wide range of operating conditions.

E. Stability
The dominant pole for an off-chip capacitor (e.g., \(C_L = 1\mu F\)) compensated LDO regulator, exists at the output node (pO in Fig. 1). As a large MP contributes the first non-dominant pole (pg) at a relative low frequency, a large equivalent series resistance of \(C_L\) (Resr) is required to generate a low frequency zero (zesr) to cancel pg. Therefore, large output variations during the load transient are induced by the large Resr. A wide output swing EA can reduce the size of the MP implying that such pole-zero cancellation is taking place at a higher frequency with a related small Resistor. Therefore, a smaller output variation during the load transient can be achieved. The second non-dominant pole (px) should be placed at a high frequency further, which implies a low resistance or low capacitance path at node VX.
III. LDO WITH THE PROPOSED APPOS CIRCUIT

However, in order to keep the phase margin above 60° without Miller capacitors, the sizes of MA11 and MA13 need to be small. Meanwhile, since the threshold voltages of the nMOSFET and pMOSFET are about 0.6 and 0.65 V, respectively, the Headroom for overdrive voltage is not enough when the supply voltage is low. Although SRG is enhanced by the class-AB operational amplifier, the improvement is still limited. To boost SRG further and enable the small-signal and large signal responses of the LDO to be best optimized with complete independence, the APPOS circuit shown in Fig. 3 is proposed. It consists of the overshoot/undershoot detection circuit and related driving circuit.

A. Overshoot and Undershoot Detection Circuits

Two complementary current comparators composed of MC1–MC4 (shown in Fig. 4) are designed to detect the overshoot and undershoot during transient state. VP and VN are the gate voltages of MA11 and MA13. The currents through MC1 and MC2 are mirrored from MA11 and MA13, respectively. In steady state, both MA11 and MA13 are in the saturation region and carry equal currents. The relationship between (W/L)N and (W/L)P satisfies that μN(W/L)N = μP(W/L)P, which means that the overdrive voltages are the same in those MOSFETs with equal currents. Since the equivalent W/L aspect ratio of MC1 is smaller than that of MC2, MC1 is in the saturation region, whereas MC2 is forced into the deep linear region in order to sustain equilibrium. That makes VOVER close to ground. Similarly, VUNDER is pushed up to near VIN. When ILOAD suddenly drops, VOUT rises rapidly, and the current through MA11 increases while that through MA13 reduces dramatically. Thus, both VP and VN decrease abruptly. Consequently, MC1 is forced to the deep linear region, and VOVER is abruptly pushed up close to VIN. Similarly, when ILOAD suddenly increases, VOUT decreases rapidly, and VUNDER is pulled down to near ground instantaneously. In the proposed complementary current comparator, the two currents are changed in the reverse direction, and the maximum driving currents are not constrained by the bias current as the conventional current comparator [11]. Meanwhile, the capacitor driven by the complementary current comparator is quite small. Hence, the bias current can be very low with a fast response time. The absolute value of the input differential voltage, at which the APPOS circuit is triggered, is set by the proportion of the Equivalent W/L aspect ratio between MC2 and MC1. Since the overdrive voltages of MA11–MA14 are almost equal, VP and VN decrease by the same amount as VOUT increases. When VP and VN drop to a particular value, MC1 and MC2 are in the Saturation region. After that, since the gain of the current comparator is very high, when VOUT continues to increase a little, VOVER increases to be close to VIN. The trigger voltage VTRIG, which is derived from both MC1 and MC2 carrying the same current in the saturation region, can be found from 12μNCOXWLNI = 12μPCOXWLPI = VOV + VTRIG (5) where M is the proportion of the equivalent W/L aspect ratio between MC2 and MC1 and VOV is the overdrive voltage of MA1–MA14 so that VTRIG = [(1−M−1)/(1+M+1)]VOV ·MC3 and MC4 function similarly. When VOUT approximately returns to the nominal value from undershoot, the bias current of LDO is higher than that from overshoot due to the effect of the adaptive biasing circuit. To counteract the VOV difference, the value of VTRIG is about 0.33 and 0.42 times that of VOV for the undershoot and overshoot, respectively. In addition, VTRIG is the proper voltage that prevents the APPOS circuit from being falsely triggered in the steady state or being prematurely turned off before the completion of the transitions.

B. Driving Circuit

The driving circuit shown in Fig. 4 is composed of MC5–MC10. MC5, and MC6, acting as two switches controlled by VOVER and VUNDER, respectively, are normally off in the steady state. Then, MC7 and MC8 turn off MC9 and MC10 during normal operation, respectively. When ILOAD suddenly decreases, VOUT rises rapidly, and the operation principle of the proposed APPOS circuit is shown in Fig. 3. As previously mentioned, once VOVER is abruptly pushed to VIN, MC5 is conducted. Since the equivalent W/L aspect ratio of MC5 is much larger than that of MC7, MC5 is pushed to the deep linear region, and the gate voltages of MC9 and MA11 are equal. The APPOS circuit injects extra current to charge the gate capacitance of MP, and the gate voltage of MP is increased to reduce ILOAD. When VOUT is approximately regulated back to the nominal value, VOVER returns to near ground. Thus, MC5 is off, and then MC7 shuts down MC9. This demonstrates the automatic on/off feature of the proposed APPOS circuit. Although MC7 divides the current from MA9 during transient state, the current through MA9 is large following the MOS square law while the current through MC7 is constant at about 0.1 μA. When VOUT is close to the normal value, MC5 is off with VOVER back to near ground. Hence, the effect of MC7 is negligible to the performance of the LDO. Similarly, as shown in Fig. 5(b), when ILOAD suddenly increases, VOUT drops rapidly, and this undershoots pulls VUNDER down to near ground. Therefore, MC6 is conducted and forced to the deep linear region. This leads the gate voltage of MC10 to equal that of MA13. Then, the APPOS circuit draws extra current to discharge the gate capacitance of MP, whose gate voltage decreases to increase ILOAD. The operation is automatically shut down again when VOUT approximately returns to the steady state. Since the response time of the APPOS circuit is reduced by complementary current comparators and the current delivered by the APPOS circuit reduces when the VOUT gets close to the final value, the APPOS circuit can thus be fully turned off before VOUT reaches the nominal value by proper designs. Hence, oscillations caused by the slew-rate enhancement circuit can be prevented in all kinds of conditions. Moreover, the dependence between the small-signal and large-signal responses is eliminated. Therefore, the transistor sizes in the operational amplifier are optimized.


http://ijesc.org/
freely with Cgsp functioning as the Miller capacitor to meet the key specifications such as GBW and phase margin. In addition, the APPOS circuit can improve the SRG significantly while only consuming very low bias currents for two complementary current comparators. Hence, the proposed LDO realizes fast-transient response with ultra low power consumption. The simulated load-transient responses shown in Fig. 4, where VIN = 1.8 V, VOUT = 1.7 V, and ILOAD switches from 100 μA to 100 mA with a 100-pF Cload, prove the transient performance improvements brought by the APPOS circuit. The APPOS circuit delivers up to a 5-μA current to charge or discharge the gate capacitance of MP, while the total quiescent current of LDO is only 1.2 μA. The undershoot, the overshoot, and the recovery time of the LDO without the proposed APPOS circuit are about 580 mV, 200 mV, and 7.8μs, respectively, while those of the LDO with the proposed APPOS circuit are about 220 mV, 200 mV, and 2.6μs only, respectively. The settling time reduces by three times. It should be noticed that, when ILOAD switches from 100 mA to 100 μA, the extra current delivered by the APPOS circuit reduces from 5 to 2.5 μA when VOUT rises and keeps to about 1.8 V. The current reduction is caused by the adaptive biasing circuit. When VOUT begins to rise, ILOAD is high, and the gate-source voltage of MA1 –MA4 is large due to the adaptive biasing circuit. However, since the bias current of MA4 reduces as ILOAD drops dramatically, the source voltage of MA1 and MA4 is increased by the flipped voltage follower. Accordingly, the gate-source voltage of MA1 decreases. Then, the current through the class-AB operational amplifier and APPOS circuit reduces.

IV. SIMULATION RESULTS
The simulations of the above all designs are carried out by using H-SPICE tool in CMOS technology. The simulated waveforms for all above circuits are shown below.

Fig.5: Simulation result for figure 2

Fig.6: Simulation results of the proposed LDO with the APPOS circuit

V. CONCLUSION
This paper presented an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low IQ, and high PSR under a wide range of operating conditions. The proposed LDO regulator was designed and fabricated using a 90-nm CMOS process to convert an input of 1.8 V to an output of 1.7-1.8 V, while achieving a PSR of ~50 dB with a 0–100-kHz frequency range. In addition, a 28-mV maximum output variation for a 0–100 mA load transient, and a 99.94% current efficiency was achieved. The experimental results verified the feasibility of the proposed LDO regulator.

VI. REFERENCES