Performance Analysis of SRAM at Different Technologies using Cadence
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Abstract:
SRAM is a type of semiconductor memory uses bi-stable circuit to store 1 bit of data. SRAM cell don’t require refresh circuits just like DRAM. The power consumed by single cell varies on the operations they perform. SRAM is a high speed memory it takes less time to access the data. Hence, it is used as a cache memory in processors and controllers. DRAM is denser compared to SRAM, they are used in main memories, where speed is not a higher part of importance. The applications of SRAM are growing wider and they are extended to industrial and automotive electronics as well. In this thesis SRAM cell is designed in two different technologies i.e., 180nm, 45nm and compared for various parameters like area, total transient power etc., all peripherals like pre-charge, Sense amplifier are designed. Layouts are created in such a manner that, they occupy minimum area. The PVT Analysis is carried out in order to check how better SRAM cell can withstand the changes and to observe the variations in power values. Power values are also compared when the width of SRAM Cell is Doubled and Tripled.

Keywords: Area, CMOS, nmos, pmos, PVT analysis, Total Transient Power.

1. INTRODUCTION

Due to extended class of personal gadgets like PC’s smart phones, audio and video based multimedia products, banking products and digital cards etc., all these products demand high-speed accessibility, high speed computations and even real time functioning capabilities. The performances of these gadgets are restricted because of their size and lifetime. One of the serious issues to be considered is IC design cost. The design engineers are working hard to develop new approaches and various design methodologies to obtain more power efficient designs which means achieving same level of performance at reduced power levels. Memory circuits are crucial parts of systems; they do contribute for total power consumptions of a system, reducing the power dissipations in memories would obviously improve power efficiency, performance, reliability & reduce over costs as well. In recent days, low power & high speed SRAMs have been a particular part of many VLSI chips. SRAM is used as cache memory, which is speedy and used to increase the speed of interaction between processor and memory interface. As the dependability on technology increased like usage of laptops, tablets and smart phones raised, they started demanding the faster access between processors and memory interfaces i.e. RAM speeds. This drove VLSI design engineers to work on low power consuming and high speed SRAM designs. In this research, we worked on the power issues and tried to obtain the comparisons of power values between various factors which are explained in further sections.

II. OBJECTIVE

The main idea of this project is to evaluate SRAM performance on the basis of power consumption, area optimization and PVT [Process variation temperature] analysis.

III. SOFTWARE

Cadence Design Systems is an electronic design automation software and engineering services company providing various types of design and testing tasks including:
Virtuoso Platform-Tools for designing integrated circuits that are fully customized include schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation.
Encounter Platform-Tools for the development of integrated digital circuits. This includes floor planning, synthesis, testing, place and route planning. Verilog netlists typically start with a digital design.
Incisive platform-Tools to simulate and functionally validate RTL including models based on Verilog, VHDL, and System C. It includes formal checking of the equivalence., hardware acceleration, and emulation. The proposed work is done in Virtuoso platform using gpdk45, gpdk180 nm technology.

IV. SRAM AND IT S PERIPHERALS

Static Random access memory (SRAM) is a type of semiconductor memory used to store "1" and "0" bits. SRAM utilizes bi-stable circuit with 2 inverters cross coupled made of Transistors/MOSFETS to store every bit. In SRAM the information is lost when the memory is not electrically charged, they are volatile. SRAM is speedy than that of DRAM. Due to its high speed SRAM is used in cache memories.

Figure 1. 6T SRAM Cell
Read Operation - The two input lines BL and BLB are precharged to vdd, the sense amplifier decides data, based on the difference obtained between 2 input lines. If ‘0’ is stored the sense amplifier output goes low and vice versa for ‘1’.  
Write Operation - In order to write 1, BL is assigned with 1 and BLB with 0, vice versa for writing 0.  
Standby Mode - In this mode, the word line is not powered, so both the access transistors are uncoupled from SRAM cell, hence in this mode memory cell retains its previous data as long as power supply is provided.  
Sense Amplifier - A sense amplifier is part of the read operation that is used when data is to be read from the SRAM cell, it senses the low power signals from the bit lines that represents data bit 1 or 0 stored in memory cell. They are used to speed up the read operation. Sense amplifier takes the small signal difference bit line voltage as input and gives full swing single ended output.

V. DESIGN METHODOLOGY

Firstly we draw schematic diagram of the given design according to that of specified requirements. Secondly the symbol is to be generated by creating test bench. Thirdly Transient, AC & DC analysis is to be done. Finally layout will be created and verification is done through DRC, LVS and QRC, followed parasitic extraction. Symbols for all these circuits are created in 2 different technologies and instantiated everytime for performing different analysis. The steps for drawing a schematic and creating symbol remain same for both the technologies. Steps for simulations also remain same. Schematic View and Symbol for SRAM cell are shown below.

VI. RESULTS AND DISCUSSIONS

Transient analysis is performed for all the cases, Analysis is performed for different W values, i.e. 1W, 2W, 3W and total transient power is obtained and compared. The design should be able to withstand any changes even in worst conditions too; Such design performances can be analyzed by Process Voltage Temperature (PVT) analysis. Corner analysis is a part of integrated Circuit design process, to be performed by varying the parameters like input voltage & temperature.
1. It is costlier compared to DRAM.

B. Disadvantages:
1. It is volatile i.e. stored data will be lost if the memory is not electrically powered.

VIII. APPLICATIONS
1. Networking.
2. Aerospace.
3. Embedded purpose.
4. In computers.
5. Medical.

IX. CONCLUSION
The present work analyzes the Power calculations and Area analyses for different widths in different technologies. In the first instance 6T SRAM cell is designed to operate under normal conditions; further analysis is carried out for different ‘W’ values in order to understand the behavior of SRAM cell. Later, PVT analysis for the 6T cell is performed because this is the heart of whole design which helps in understanding the variations in power consumption of memory cell for variations in Process, Temperature and Voltages. Finally, Layout of particular cell is drawn in a formal way, so that the area of layout is minimized which results in reduction of power dissipation.

X. FUTURE SCOPE
Higher memories of order MBs and GBs can be designed and analyzed, Noise Margins and delays can be calculated by using various methods, and drawing layouts for bigger memories can be simplified by using Scripting languages like SKILL, PERL etc., SRAM density has grown substantially, it holds an application in automotive industries too, It is becoming a crucial part of system-on-chips (SoCs). In concern to all these issues, the further course of actions involve in reduction of leakages in SRAM cell.

XI. REFERENCES


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Table.1. Total Transient power values for different widths in 180nm

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Total Transient Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1W</td>
</tr>
<tr>
<td>Read1</td>
<td>2.0552μW</td>
</tr>
<tr>
<td>Write0</td>
<td>289.27μW</td>
</tr>
<tr>
<td>Read 0</td>
<td>2.0552μW</td>
</tr>
</tbody>
</table>

The appropriate power values for different analysis in 180nm are shown in above tables. Read power for 0 & 1 remain approximately same.

Table.2. Total Transient power values for PVT analysis in 180nm

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Total Transient Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(P= FF, V= 1.98, T= -40°)</td>
</tr>
<tr>
<td>Write1</td>
<td>1.509μmW</td>
</tr>
<tr>
<td>Read1</td>
<td>2.0108μmW</td>
</tr>
<tr>
<td>Write0</td>
<td>1.5569μmW</td>
</tr>
<tr>
<td>Read 0</td>
<td>2.7289μmW</td>
</tr>
</tbody>
</table>

Table.3. Total Transient power values for different widths in 45nm

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Total Transient Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1W</td>
</tr>
<tr>
<td>Read1</td>
<td>55.81μW</td>
</tr>
<tr>
<td>Write0</td>
<td>28.272μW</td>
</tr>
<tr>
<td>Read 0</td>
<td>55.808μmW</td>
</tr>
</tbody>
</table>

Table.4. Total Transient power values for PVT analysis in 45nm

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Total Transient Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(P= FF, V= 1.98, T= -40°)</td>
</tr>
<tr>
<td>Write1</td>
<td>68.887μmW</td>
</tr>
<tr>
<td>Read1</td>
<td>209.963μmW</td>
</tr>
<tr>
<td>Write0</td>
<td>319.36μmW</td>
</tr>
<tr>
<td>Read 0</td>
<td>119.396μmW</td>
</tr>
</tbody>
</table>

Table.5. Area consumed by single SRAM cell

<table>
<thead>
<tr>
<th>Technology (ηm)</th>
<th>Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>138.334</td>
</tr>
<tr>
<td>45</td>
<td>2.741</td>
</tr>
</tbody>
</table>

We can observe a drastic reduction of area in 45nm when compared to that of 180nm, which in turn reduces the total power consumption. We can conclude that reduction in technology can reduce area and power.

VII. ADVANTAGES & DISADVANTAGES

A. Advantages:
1. It does not need to refresh memory contents. And therefore no refresh logic circuit is used.
2. Performance
3. Reliability
4. Low power consumption

B. Disadvantages:
1. It is costlier compared to DRAM

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[13]. Jing Guo, Lei Zhu, Yu Sun, Huiliang Cao, Hai Huang, Tianqi Wang, Chunhua Qi, Rongsheng Zhang, Xuebing Cao, Liyi Xiao, and Zhigang Mao, “Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications” in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.