Voltage Regulation of Single Phase Supply with the Help of Matrix Converter using FPGA

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Abstract:
The paper presents a single phase matrix converter whose output is controlled by means of a digital phase locked loop. The digital phase locked loop is implemented by means of a FPGA using VHDL language. Here the DCO is replaced with an analog to frequency converter IC. The output waveform of the digital phase locked loop is visualized using Xilinx software whereas that of matrix converter using Matlab/Simulink.

Keywords: Matrix converter, Digital Phase Locked Loop

I. INTRODUCTION

Matrix converter is one which converts fixed ac voltage having fixed frequency to variable ac output. Here the RMS value of the input voltage applied to the load circuit is changed by introducing thyristors between the load and the constant voltage. The RMS value of the ac voltage is varied by controlling the triggering angle ‘α’ of the thyristors employed in the circuit. There are two different types of thyristor control used in practice to control the ac power flow. 1. On-Off control

2. Phase control. Matrix converter consists of four bidirectional switches, two antiparallel MOSFETs per switch. These bidirectional switches are capable of conducting current in both directions, blocking forward and reverse voltages. The method eliminates the use of electrolytic capacitors. It has several advantage including sinusoidal output voltage and input current, unity input power factor, inherent regenerative capability. The output is controlled with the help of digital phase locked loop. The various components employed in the construction of the digital PLL are phase/frequency detector, low pass filter, and a DCO. Here the DCO is replaced with a voltage to frequency detector IC. The phase detector converts the phase difference error to a numerical value that can be processed digitally by the loop filter. The loop filter regulates the control signal values as per the difference error values. The control signal values applied to PWM generator as its count values. The PWM generator produces the signal which controls the load voltage from its duty cycle. The duty cycle of PWM changes as per error signal values produced by phase comparator system. The input to the IC is the voltage across the load and the output from the IC is compared with the reference clock signal given as input to the phase/frequency detector. The digital PLL is implemented with the help of FPGA using VHDL language. FPGA doesn’t have a fixed hardware structure, and is programmable according to user applications.

II. PRINCIPLE OF OPERATION

The Single Phase Matrix Converter (SPMC) is composed of the four-switch S1 - S4 connecting the single-phase input to the single-phase output. The instantaneous input voltage is \( v_i(t) \) following as

\[ v_i(t) = v_{in}\cos(\omega t) \]

The instantaneous input current is \( i_i(t) \)

Model 1: \( i_i(t) = + i(t); \ S1=S4=ON & S2=S3=OFF \)

Model 2: \( i_i(t) = - i(t); \ S1=S4=OFF & S2=S3=ON \)

Model 3: \( i_i(t) = 0 \ S1=S4=OFF & S2=S3=ON \)

The instantaneous output voltage is \( V_o(t) \)

Mode 1: \( V_o(t) = + V_o(t); \ S1=S4=ON & S2=S3=OFF \)

Mode 2: \( V_o(t) = + V_o(t); \ S1=S4=OFF & S2=S3=ON \)

Mode 3: \( V_o(t) = 0 \ S1=S4=OFF & S2=S3=ON \)

Where \( V^k(t) = output \) voltage during any cycle \( k \)

\[ V^k(t) = \text{input voltage during any cycle } k \]

The modulation indexes of every switch during any switching time is given by

\[ m_j^k = \frac{\Delta_j}{T_2} \]

\[ \sum_j m_j^k = 1 \]

Where

\( m_1 \), \( m_2 \) = The modulation index of PWM signals during any cycle \( k \)

\( \Delta_j \) = The time interval when the circuit is in mode \( j \), during the \( k \) th cycle,

\( j = 1, 2 \)

\( T = 1/F_s \) = Switching cycle time.

III. WORKING

The working of the matrix converter
The ac input voltage is applied to all the MOSFETs. The MOSFETs are chosen such that the breakdown voltage and reverse blocking voltage must be sufficient for the MOSFETs to operate properly without getting damaged. The output voltage depends upon the current flow through the load. To get a positive output voltage, the current is allowed to pass through the load in one direction and to obtain a negative output voltage the current is allowed to flow in the other direction. As stated in the introduction of the matrix converter it consists of 8 MOSFETs. Each pair will be connected in anti-parallel with the other one. Let s1, s2, s3, s4 be the name of each pair. At the start the MOSFETs are in off state. As MOSFETs are voltage controlled device some amount of voltage must be given to the gate to bring the MOSFETs into on state. During the positive half supply of the ac input voltage the device whose drain is connected to the ac supply from s1 and s4 are turned on by means of applying a threshold voltage to its gate. The MOSFETs get turned on and the supply flows across the load. During the negative half supply of the input voltage the opposite switches of the same pair (s1 & s4) are switched on by pwm means. To restrict the maximum amount of voltage given to the load pwm is used. During the positive half supply of the ac input voltage the device whose drain is connected to the ac supply from s2 and s3 are turned on by means of applying a threshold voltage to its gate. The MOSFETs get turned on and the supply flows across the load. During the negative half supply of the input voltage the opposite switches of the same pair (s2 & s3) are switched on by pwm means. To restrict the maximum amount of voltage given to the load pwm is used.

IV. DIGITAL PHASE-LOCKED LOOP

Digital Phase-locked loop has been intensively used in control application system where accurate frequency synchronization is required. In its basic blocks of digital phase-locked loop consists of a phase frequency detector (PFD), a loop filter and a digital-controlled oscillator (DCO) as all blocks of PLL are digital so it is called as All digital PLL as shown in Figure 2. The DCO output signal is compared with the reference signal by the PFD, which produces an error signal to indicate the phase difference values. The phase error signal is filtered by the loop filter to providing a control signal value proportional to the phase difference between the two signals. This control signal value is used to vary the DCO frequency in such a direction that reduces the phase difference. An equilibrium state is reaches when the DCO frequency is exactly equal to the frequency of the reference input signal. By inserting a frequency divider (usually a digital programmable counter) in the feedback path the DCO frequency can be synchronized to a multiple of the reference frequency. Such a configuration is called a frequency synthesizer, which is usually used to generate precise frequencies in communication systems. The range of frequencies from minimal to maximal value from its reference where the DPLL will remains in the locked condition is called the lock range of the DPLL. If the PLL is initially locked and input signal frequency becomes smaller than $f_{min}$, or if input signal frequency exceeds $f_{max}$, the PLL fails to keep the it’s rated speed equal to reference input signal frequency, and the PLL becomes unlocked. The PLL basic configuration or the frequency synthesizer configuration can be used, in which the DCO is replace by voltage to frequency converter which generates a pulse train of frequency proportional to load voltage.
V. BLOCK DIAGRAM

VI. DESCRIPTION

The thyristors employed in the circuit can be switched on only if its gate is triggered. The triggering action is performed with the help of FPGA. A digital phase locked loop is implemented in fpga. In general the various components in the loop includes phase detector, digital low pass filter and a DCO. Here the DCO is replaced with a voltage to frequency IC AD7740. The output voltage is first stepped down and then rectified. The output of the rectifier is given as input to the IC. The IC converts the input voltage into its corresponding frequency. The output Frequency is fed back to the fpga as input. Closed loop action is implemented here.

VII. SOFTWARE DESCRIPTION

7.1 MATLAB SIMULINK

Simulink, developed by MathWorks, is a graphical programming environment for modeling, simulating and analyzing multidomain dynamic systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in automatic control and digital signal processing for multidomain simulation and Model-Based Design.
7.2 SIMULATED MODEL

![Simulated Model](image)

Figure.4. Simulated Model

7.3 SIMULATED OUTPUT

![Simulated Output](image)

Figure.5. Simulated Output

7.4 XILINX DESCRIPTION

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the ModelSim logic simulator is used for system-level testing. Other components shipped with the Xilinx ISE include the Embedded Development Kit (EDK), a Software Development Kit (SDK), and ChipScope Pro.

7.4 XILINX SIMULATED OUTPUT

![Xilinx Simulated Output](image)

Figure.6. Xilinx Simulated Output

VIII. CONCLUSION

Converters generally require a dc link for conversion. With the implementation of this project the need for a dc link can be eliminated. Moreover, the input-output currents are nearly sinusoidal wave when the switching frequency and modulation index are increased. From these results, these can be further employed in voltage controllers of single phase power supply and several other applications like controlling the input supply given to an inductor motor.
X. REFERENCE


