Design and Analysis of an Efficient Power and Area Magnitude Comparator Using GDI at 130nm

D.Imran¹, S.Rambabu²
M.Tech, VLSI System Design¹, Assistant Professor²
Department of ECE
Santhiram Engineering College, Nandyal, Kurnool, A.P, India

Abstract:
As per recent trends of miniaturization in chip sizes, VLSI design has become a very important research area. In VLSI technology, silicon area, power consumption and propagation delay are the major design issues which play vital role in it. In today's world, the demand of portable devices is increasing day by day. Thereby, it is required to fabricate more number of devices on a small silicon area in order to reduce the size of the devices. The main factors on which the portability and popularity of these devices depends are area, number of transistors used to implement basic functionality, power dissipation, speed and reliability. Comparators are basic design element in digital VLSI design, digital signal processors (DSP) and data processing application-specific integrated circuits (ASIC). Comparator is eminent to be an extremely basic and useful component of arithmetic units of the digital systems. In which, a magnitude comparator design is carried out based on different low power CMOS techniques and compare all them with proposed technique based on different low power parameters. The proposed GDI one of the technique which helps in designing low-power digital combinatorial circuit with less number of transistors. Due to reduction in transistor count, it also allows in reducing power consumption, propagation delay which in turn increases the speed of the circuit, and area of digital circuits while maintaining low complexity of logic design. The simulation is carried out at 130nm technology.

Keywords: Power consumption, CMOS Low power techniques, GDI, Full adder, magnitude comparators, Scaling techniques.

I. INTRODUCTION
Comparator is a basic module in the arithmetic logical unit of digital signal processors and application specific integrated circuits used in various digital electronic devices. In the world of technology the demand of portable devices are increasing day by day. Demand and popularity of these devices depends on the small silicon area, higher speed, longer battery life and reliability. The system performance can be affected by enhancing the performance of the comparator circuit used in these systems. Power and area consumption is a key limitation in many electronic devices such as mobile phone and portable computing systems etc. So far several logic styles have been developed to improve area and power consumption. Several new logic styles have been developed that have better performance as compared to the traditional CMOS logic styles. The performance estimation of full adder is based on the design criteria for specific application. The main issues in performance estimation are Area Consumption, Power dissipation, Propagation delay and Power –Delay Product. Area, speed and power consumption are the main criteria of concern in CMOS Comparator design which often conflict with the design methodology and act as constrain on the design of comparator circuits. These performance criteria’s should be individually investigated, analyzed for the various designs of the comparator by different logic styles. Due to the growth of CMOS technology the VLSI industry has been driven toward the design of system on chip. Demand of the area efficient devices has been increased due to the explosive growth of VLSI industry. As Comparator is one of the basic circuitry used in arithmetic unit of various portable devices so area efficient comparator can help in the fulfilment of these demands. Due to this area efficient design of comparator has become essential for the researchers. Area of the circuit mainly depends on three things: Number of transistors in the circuit, Feature size of the transistor and Wiring complexity. No of transistors is of course the primary concern in the area efficient design because it affects the complexity of any circuit. Power dissipation in any full adder circuit depends on two components: One is static dissipation which occurs due to the leakage current or other current drawn continuously from the power supply and second is dynamic dissipation which occurs due to switching of transient current, and charging and discharging of load capacitances. The static power dissipation is the product of the leakage current and supply voltage. In which the 4-bit magnitude comparator is implemented based on GDI Based Full adders, NOR and AND gates shown in below modules.

II. COMPARISION OF PERFORMANCE OF DIFFERENT FULL ADDERS
Full Adder is developed to overcome the drawback of Half Adder circuit. It can be add two one-bit numbers A and B, and carry. The full adder is a three input and two output combinational circuit.

FIGURE 1. FULL ADDER
In which, Full adder is implemented based on different low power techniques like Basic CMOS, Transmission gates, 12T, 10T Pass transistors and Gate Diffusion gate (GDI) shown in below.

**A) CMOS based FULL ADDER:**

The below diagram signifies the CMOS based full adder, In which that required 28 Transistors to built one-bit Full adder shown in below.

![CMOS Based Full Adder Diagram](image1)

**B) TRANSMISSION BASED FULL ADDER**

From the above fig, that signify more no of transistors to built one full adder. Hence that occupy large area and provide more power dissipation. To overcome this, we go for transmission based full adder that requires 20 transistors to built full adder.

![Transmission Based Full Adder Diagram](image2)

**C) 12T PASS TRANSISTORS BASED FULL ADDER**

From the above fig, that signifies transmission based one-bit full adder require more no of transistors to built one full adder. Hence that occupy large area and provide more power dissipation. To overcome this, we go for 12T Pass transistors shown in below.

![12T Pass Transistors Diagram](image3)

**D) 10T PASS TRANSISTORS BASED FULL ADDER**

From the above fig, that signifies 12T Pass transistors based one-bit full adder require more no of transistors to built one full adder. Hence that occupy large area and provide more power dissipation. To overcome this, we go for 10T Pass transistors shown in below.

![10T Pass Transistors Diagram](image4)
From the above fig, that signifies 10T Pass transistors based one-bit full adder require more no of transistors to built one full adder. Hence that occupy large area and provide more power dissipation. to overcome this, we go for GDI Low power technique based full adder that require only 8 Transistors to built one bit full adder shown in below.

**D) PROPOSED GDI LOW POWER TECHNIQUE BASED FULL ADDER**

*Gate Diffusion Input* is a New Existing Method to reduce power dissipation, propagation delay with less. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors shown in below.

![Figure 6. Basic GDI Cell](image)

**Table 1: Instruction of Basic GDI Cell**

<table>
<thead>
<tr>
<th>S.No.</th>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>B</td>
<td>A</td>
<td>A'B</td>
<td>F1</td>
</tr>
<tr>
<td>2</td>
<td>B</td>
<td>1</td>
<td>A</td>
<td>A'+B</td>
<td>F2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>B</td>
<td>A</td>
<td>A+B</td>
<td>OR</td>
</tr>
<tr>
<td>4</td>
<td>B</td>
<td>0</td>
<td>A</td>
<td>AB</td>
<td>AND</td>
</tr>
<tr>
<td>5</td>
<td>C</td>
<td>B</td>
<td>A</td>
<td>A'B+AC</td>
<td>MUX</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>A</td>
<td>A'</td>
<td>NOT</td>
</tr>
</tbody>
</table>

In which, full adder is designed with 2-4 T XOR Gates and 2to 1 MUX. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design. But it adds noise in output logic levels by effect off delivered leakage power when transistor is off and degrades the performance of the system. the below fig signifies GDI based full adder that required only 8 transistors to built one bit full adder.

![Figure 7. GID Based full adder](image)

From the above discussion, by comparing all full adders, The GDI based Full adder is the best technique to built electronic circuits. hence in which, the proposed comparator is implemented based on GDI shown in below.

**III.PROPOSED 4-BIT MAGNITUDE COMPARATOR BASED ON GDI**

**A) 1-BIT MAGNITUDE COMPARATOR**

Digital Comparator “also called Magnitude Comparator” is a combinational circuit that compares two inputs binary quantities (A and B) and generates outputs to indicate whether the inputs are equal or which input is greater than the other, therefore, the circuit has three outputs to indicate whether A=B, A>B or A<B. At any given input quantities, only one output should be equal to logic ‘1’.

![Figure 8. Block Diagram of n-Bit Magnitude Comparator](image)

Fig. shows a block diagram of the magnitude comparator. The circuit, for comparing two n-Bit numbers, has 2n inputs & 22n entries in the truth table, for 2-Bit numbers, 4 inputs & 16 rows in the truth table, similarly, for 3-Bit numbers 6 inputs & 64 rows in the truth table.
Table 1. Truth table of 1-bit Comparator

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

B) 4-BIT MAGNITUDE COMPARATOR

The below fig signifies 4-bit magnitude comparator simple block diagram and its internal diagram based on full adders, NOR and gates designed based on low power GD1 Technique shown in below.

Figure 9. Simple diagram of 4-bit magnitude comparator

Figure 10. Symbolic representation of 4-bit magnitude comparator

Figure 11. Internal diagram of 4-bit magnitude comparator based on GD1

The above fig signifies the 4-bit magnitude comparator based on GD1 that implemented based on 6 GD1 based full adders, 3 GD1 based AND & 3 GD1 based NOR gates shown in above fig.

IV. RESULT AND ANALYSIS

The above all schematic diagrams are simulated based on MICROWIND tool, the below fig signifies the layout and simulated waveforms of proposed 4-bit magnitude comparator based on GD1.

Figure 12. Layout of proposed 4-bit magnitude comparator based on GD1
The below table signifies the comparison of different low power full adders in terms of power dissipation, area and delay, no of transistors shown in below table.

<table>
<thead>
<tr>
<th>Type of Technique</th>
<th>No of Transistors</th>
<th>Power Dissipation</th>
<th>Area</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Full adder</td>
<td>28</td>
<td>16.925mW</td>
<td>62x80μW</td>
<td>18ps</td>
</tr>
<tr>
<td>TG Full adder</td>
<td>20</td>
<td>14.27μW</td>
<td>44x10μW</td>
<td>27ps</td>
</tr>
<tr>
<td>12T Pass Full adder</td>
<td>12</td>
<td>16.461μW</td>
<td>23x9μW</td>
<td>19PS</td>
</tr>
<tr>
<td>10T Full adder</td>
<td>10</td>
<td>7.52μW</td>
<td>28x38μW</td>
<td>15PS</td>
</tr>
<tr>
<td>GDI Full adder</td>
<td>8</td>
<td>0.45μW</td>
<td>20x7μW</td>
<td>12PS</td>
</tr>
</tbody>
</table>

Table 1: Comparison of different low power full adders

From the above table, we conclude that the Low power GDI Technique is the best to design complex electronic circuits and the below table signifies the power dissipation, area and delay and no of transistors require to built 4-bit magnitude comparator based on GDI.

V. CONCLUSION

The GDI technique has been presented and it has been shown how it makes use of lesser number of gates to design a circuit which is desirable for fast and low power applications. The comparison between GDI and CMOS techniques has also been depicted and experimental delay Area and power dissipations values of both have also been produced. This technique can be successfully applied to larger digital circuits like comparators, multipliers, adders, etc.

VI. REFERENCES


[3] Etienne Sicard, Sonia Delmas Bendhia, Basic of CMOS Cell Design, TATA Mc GRAW-HILL.

