Low Power 8 Bit ALU for Internet of Things (IoT) Processor

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Abstract:
This research work proposes novel low power ALU for IOT applications. This paper briefly about the significance of datapath components in achieving the low power constraint. Here the datapath architectural optimizations are done at the gate level implementation for the processors used in IoT applications. Arithmetic logic unit (ALU) of the IoT processor was designed with low power datapath components to reduce the power consumption while still improving the design performance. Standard ASIC design methodology was utilized for gate level implementations with 65nm technological node. The proposed datapath architectural optimization for ALU design has resulted in 25.1\% less leakage power with 30.5\% better performance and 37.8\% less area. From this study we have come across that the proposed concept can be applied to designs to achieve the desired design constraints.

Keywords: IoT, ALU, Reversible logic gates, Datapath.

I. INTRODUCTION
Low power circuit design has now become an important subject of interest, which is evident from the surge of related activities in the engineering and research domain. In the past, the device density and operating frequency were low enough that the power dissipation was not a constraining factor in the chips. However, as the scale of integration improves, more transistors are being packed into a chip that leads to an increase in the processing capacity of chips and thereby results in the increase of power dissipation. Earlier the major concerns among researchers and designers for designing integrated circuits were on area, speed, and cost; while secondary importance was paid to power dissipation. In recent years, however, this scenario has changed and now reducing power dissipation through improved circuit design techniques is an important research area.

With the increasing demand of battery operated portable systems, it is important to increase the battery life as much as possible, since it is the limited battery lifetime that typically imposes strict restriction on the overall power dissipation of such systems. Although the battery industry has been making efforts to develop batteries with a higher energy capacity, however a revolutionary increase in the energy capacity does not seem imminent. In the absence of low power circuit design techniques, present and future portable systems will either suffer from a very short battery life or a very heavy battery pack. So, portable systems that are powered with batteries require low power circuit design for increasing their lifetime. Low power circuit design is highly desirable for burst mode type systems, where computation occurs only for short duration, and the system is inactive for the majority of time. For such type of battery operated systems, it is highly unacceptable to have excessive drainage of useful battery power during the long standby period. To integrate more functions on a chip, the feature size of a transistor has to shrink. As a result, the power dissipation per unit area rises, which increases the chip temperature. Since the dissipated heat needs to be removed to maintain an acceptable chip temperature, large cooling devices and expensive packaging techniques are required in portable devices and high-performance digital systems such as microprocessors. The issue of reliability of an electronic system with the increase in system temperature also accelerates the need for low power circuit design. High power dissipation systems often run hot, and the high temperature tends to accelerate the silicon failure mechanism. Another major demand for low power circuit design comes from environmental concerns. Modern offices are now furnished with office automation equipment’s that consume large amount of power. Since electricity generation is a major source of air pollution, inefficient energy usage by electronic equipment indirectly contribute to an increase in the environmental pollution. The requirement for low power circuit design varies from applications to applications. In case of battery operated portable systems, the overall goal of reducing the power dissipation is to keep the battery lifetime and weight reasonable; and for high performance and non-battery operated systems, the overall goal of power minimization is to reduce the overall system cost (cooling, packaging and energy bill) and also to increase the system reliability. Hence, reducing the power dissipation in electronic systems by utilizing low power circuit design is becoming a top priority issue.

Internet of Things (IoTs) is a concept where variety of things/objects are connected to each other through wireless or wired connections and unique addressing schemes are able to interact with each other and cooperate with other things/objects to create new applications/services and reach common goals. In this context the research and development challenges to create a smart world are enormous. A world where the real, digital and the virtual are converging to create smart environments that make energy, transport, cities and many other areas more intelligent.

The goal of the Internet of Things is to enable things to be connected anytime, anyplace, with anything and anyone ideally using any path/network and any service.

The typical IOT system is depicted in fig 1. It consists of three subsystems:
- Sensor: To collect the data from the device
- Controller: To process the sensor data.
- Communication: To transmit the processed data & to transmit.


http://ijesc.org/
The controller forms the major subsystem of the IOT device. The primary requirement of the IOT device is the Ultra Low power consumption since the device will be used in remote locations & may not have power source. Existing solutions use off the shelf controllers which are primarily designed for generic high performance applications.

The other sections of the paper are organized as follows. Section II describes the motivation, section III shows the importance of reversible logic gates. The various components of ALU and their implementations and gate level architectural optimizations are characterized in section IV. Implementation and performance evaluation of simulation results are discussed in section V. Finally section VI concludes the work and the next Section gives references for the work.

II. MOTIVATION

Reversible logic based design is one of the promising low power research technologies and find its application for low power CMOS design, cryptography and digital signal processing etc. Energy dissipation is one of the major factors in IC technology. The energy dissipated in a system is directly related to number of bits lost during logical computation. This irreversible technology will dissipates loss of heat. Some information will be lost for every bit of transition; once information is lost, it can’t be recovered back [8]. Thus we can overcome this problem by considering the circuit, which is built using reversible logic [9].

III. REVERSIBLE LOGIC

Reversible logic design is one of the emerging concepts in the research field. Applications in quantum, optical, CMOS and Nano-technologies have sparked the interest towards reversible logic. Its applications are also extended to thermodynamics and adiabatic CMOS technologies. The reversible logic based design performs extreme low power dissipation and that too independent to the underlying technology. The KTln2 joules of energy dissipation in a circuit can be avoided if the circuits are designed based on reversible logic gates [9]. In both the directions reversible logic gate computes in the running process of the system. Reversible logics generate unique output vectors from the input vectors and vice versa so that they can have one-to-one correspondence between the input and outputs [11]. Typically reversible logic gate consists of k-inputs and k-outputs where output pattern is generated by mapping each possible input pattern. They are popularly denoted as k*k gates and it must produce one extra unwanted output usually called as garbage output. General expression (1) gives the reversible logic gates input vector realization,

\[ I_v = \left( I_{i_1} + I_{i_2} + \ldots + I_{i_k} + I_{j_1} + I_{j_2} + \ldots + I_{j_k} \right) \]  

(1)

and similarly expression (2) gives the output vector realization.

\[ O_v = \left( O_{i_1} + O_{i_2} + \ldots + O_{i_k} + O_{j_1} + O_{j_2} + \ldots + O_{j_k} \right) \]  

(2)

IV. ALU

A. Complex Gates:

Common forms of complex logic gates are **and-or-invert** (AOI) and **or-and-invert** (OAI) gates, both of which implement sum-of-products/product-of-sums expressions. The function computed by an AOI gate is best illustrated by its logic symbol, groups of inputs are ANDed together, then all products are ORed together and inverted for output. An AOI-21 gate, like that shown in the fig 6, has two inputs to its first product and one input (effectively eliminating the AND gate) to its second product; an AOI-121 gate would have two one-input products and one two input product.

AO22D1:

![Diagram for AO22D1](http://ijesc.org/)
AOI21D1:

![Diagram for AOI22D1](image)

Fig 6: Diagram for AOI22D1

B. Proposed Fredkin gate:

Here the Fredkin gate is designed using two AOI22D1 complex gates. This proposed Fredkin gate is used in the ALU design instead of Conventional Fredkin gate.

![Proposed Fredkin Gate](image)

Fig 7: Proposed Fredkin Gate

C. Proposed XOR gate:

The proposed Xor gate is designed using one NOR gate and one AOI21D1 complex gate. This proposed Xor gate is used in designing of the reversible gates instead of conventional Xor gate.

![Proposed XOR gate](image)

Fig 8: Proposed XOR gate

D. Adder/Subtractor:

Several types of adders are used in computing systems. A ripple carry adder has the simplest structure. In a ripple carry adder, full adders connected in series generate the sum and the carry outputs based on the addend bits and the carry input. The disadvantage of a ripple carry adder is that the carry has to propagate through all stages.

- **Half Adder/Subtractor:**

Reversible half adder/subtractor logic is implemented with the four reversible gates of which two are Fredkin and two are Feynman gates. The numbers of garbage outputs are three, garbage inputs are two and quantum cost is twelve. This implementation is as shown in fig 9. This half adder/subtractor is used in implementing four-bit parallel reversible adder/subtractor unit.

- **Full Adder/Subtractor:**

In this design the main functionality of addition and subtraction is realized by using only TR gates. Feynman gates are used for input signal buffering. The design utilizes 3 TR gates and 6 Feynman gates, in total 9 gates. The garbage output in this design is 7 and the garbage inputs are 5. The quantum cost for the design is 24. Even though one additional Feynman gate (C-NOT Gate) is used in this design, a quantum cost advantage of 4 is obtained. This quantum cost advantage is mainly due to the realization of arithmetic blocks of adder and subtractor is realized with 3 TR gates.

![Logic implementation of reversible Half Adder/Subtractor](image)

Fig 9: Logic implementation of reversible Half Adder/Subtractor

![Logic implementation of reversible Full Adder/Subtractor](image)

Fig 10: Logic implementation of reversible Full Adder/Subtractor

- **Eight-Bit reversible Parallel Adder/Subtractor unit:**

A eight-bit reversible parallel adder/subtractor is built using the full adder/subtractor and half adder/subtractor units. The figure for the eight bit adder/subtractor is shown fig 11.

![Eight bit reversible Parallel Adder/Subtractor](image)

Fig 11: Eight bit reversible Parallel Adder/Subtractor

E. Baugh Wooley Multiplier

Baugh-Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands are represented in 2’s complemented form. Partial Products
are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh-Wooley Multiplier operates on signed operands with 2’s complement representation to make sure that the signs of all partial products are positive.

![Baugh Wooley Multiplier](image)

**Fig 12: Baugh Wooley Multiplier**

**F. Incrementor**

The binary incrementor increases the value stored in the register by ‘1’. Here the Incrementor is designed using the full adder. Full adder is designed using the proposed fredkin gate.

![Incrementor](image)

**Fig 13: Incrementor**

**G. Decrementor:**

The binary decrementor decreases the value stored in a register by ‘1’. For this we can simply add ‘1’ to each other bit of the existing value stored in a register. This is basically the concept of two’s complement used for subtraction of ‘1’ from the given data. Here the decrementor is designed using the full adder. Full adder is designed using the proposed fredkin gate.

![Decrementor](image)

**Fig 14: Decrementor**

**H. Counters**

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

In practice, there are two types of counters:
- Up counters, which increase (increment) in value
- Down counters, which decrease (decrement) in value.

Here up-counter and down-counter is implemented by using incrementor and decrementor and with D-flip flops at the output. The incrementor and decrementor used are shown in Fig 13 and 14 respectively. Block diagram for up-counter and down counter are shown in Fig 15 and 16 respectively.

![Up Counter](image)

**Fig 15: Up Counter**

![Down Counter](image)

**Fig 16: Down Counter**

**L. ALU**

The ALU consists of Adder/Subtractor, Multiplier, Incrementor, Decrementor, Up Counter, Down Counter and Basic Gates. The 8 bit ALU block diagram is shown in Fig 17.

![ALU](image)

**Fig 17: 8 bit ALU**

**V. RESULTS AND OBSERVATION**

The low power Arithmetic Logic Unit for IOT processor has been designed with low power architectures to achieve minimal power consumption. Critical datapath components were identified in the processor and low power datapath
optimizations were applied to datapath blocks rather than the entire system. The proposed architectures were implemented based on Top-Down design methodology. The Design was modelled using Verilog, Functionally verified using Modelsim & mapped to 65-nm Technology library using Synthesis tool. The proposed architectural optimizations were demonstrated using the cadence RTL compiler.

Table 1 gives the results of the ALU with conventional and proposed compressor architectures. It shows that the proposed architecture has outperformed the conventional architectures in all the design parameters. As mentioned in the previous? that the proposed architecture was built with prime consideration of leakage power reduction and the Table 1 displays the exact outplay of the proposed architecture. It has reduced 25.1 % of leakage power compared to existing architecture. It has also utilized 37.8% less area and process 30.5% faster than the conventional ALU architecture.

<table>
<thead>
<tr>
<th>Leakage power (nw)</th>
<th>Implemented ALU</th>
<th>Proposed ALU</th>
<th>% change</th>
</tr>
</thead>
<tbody>
<tr>
<td>31722.296</td>
<td>23743.518</td>
<td>25.1</td>
<td></td>
</tr>
<tr>
<td>Dynamic power (nw)</td>
<td>81990.843</td>
<td>65747.669</td>
<td>19.8</td>
</tr>
<tr>
<td>Timing (ns)</td>
<td>7676</td>
<td>5334</td>
<td>30.5</td>
</tr>
<tr>
<td>Cell area</td>
<td>3173</td>
<td>1972</td>
<td>37.8</td>
</tr>
</tbody>
</table>

VI. CONCLUSION AND FUTURE WORK:
In this paper, a low power ALU for IOT applications has been illustrated using industry standard ASIC design methodology. The leakage power improved datapath architectural optimizations were proposed for IOT processor especially for battery powered devices running with lower technological node cells where leakage power is one of the primary design constraint. Further analysis of the proposed architecture suggests that the proposed datapath architectural optimizations are unique & generalized since they can be applied to any abstraction level in the design cycle and for any bit width.

Additional optimizations can be done at the transistor level designs by exploring the low power design methodologies effectively. The transistor level optimizations will further improve the power optimizations since there is scope to further optimize by using proposed architectures.

VII. REFERENCES: