Analog CMOS Implementation of Memory Units and Memory Devices

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Abstract:
The most widely used semiconductor memory types are the dynamic random access memory and static random access memory competition among memory manufactures drives the need to decrease power consumption and reduce the probability of read failure. The concept of CMOS implementation (schematic design) of different memory units and devices. Memory design is one of the interesting subject in semiconductor technology for storing binary data in large quantities. The proposed memory design takes into account the type of memory unit that is preferable for a given technology and application and is a function of required memory size. The time it takes to access the memory data, pattern and configuration to optimize the memory architecture for low power dissipation and more importantly over all system requirements. The project is dealt with basic memory architecture and their essential peripheral blocks. It emphasis on the working of memory units (eg. flip-flop) and memory devices (SRAM & DRAM) with their schematic diagram to obtain their characteristic. Memory design is one of the interesting subjects in semiconductor technology. They have fascinated world through storage of data values and program instructions. Memory is a portion of a system for storing binary data in large quantities. Type of memory unit that is preferable or a given technology is governed by its architecture and other essential building blocks. Cell structure and topology is governed by the technology (Here 300 nm, 2 metal layer C5 process). The peripheral blocks include the address decoders, sense amplifiers, voltage references, drivers, buffers, timing and control. In this design we will be defining our memory size in bits (that are equivalent to the number of cells.) The proposed size of the array is 64 bits i.e. 8 x 8 arrays. Moreover this CMOS memory design will also be including sensing amplifiers and circuits, row and column decoders, control circuitry and finally the operation of memory cells themselves. Initially memory design procedure will be primarily consisting of defining the architecture and then laying out respective memory cell. Then according to architecture the peripheral circuitry is laid out. Finally memory check and optimization procedures are carried out with various simulation tools.

Keywords: Semiconductor Memory, DRAM, Cell, Array, Spice, layout, Sense amplifiers, Decoder, Bitlines, Wordlines.

1. INTRODUCTION
The semiconductor industry is trying to catch up with Moore’s law by scaling the devices namely microprocessors and memories. Reduction in size guarantees reduction of its parasitic mainly capacitance.

The parasitic mainly contribute to increment of size and unnecessary power dissipation in the overall device as a well designed layout of chip ensures quality of work and better performance. Today memory circuits come in the form of SRAM, DRAM, ROM, EPROM, E2ROM, Flash and FRAM. Each of them has different cell designs, their basic structure, and organization and access mechanisms.

Semiconductor memory is classified on the basis of functionality, access patterns and nature of storage mechanism. There are numerous numbers of aspects in memory design namely memory cells, memory arrays, peripheral circuitry, sense amplifiers, storage density and overall reliability. Memory is classified on the basis of functionality, access patterns and nature of storage mechanism. The Read Write memory structures have read write capability and comparable access times. They are also called flexible memories and data stored as flip-flops and capacitor charge. In computer terms memory refers to RAM or ROM

2. CMOS STRUCTURE-
The CMOS (complementary metal oxide semiconductor) integrated circuit (IC) design process (the design of "chips"). CMOS is used in most very large scale integrated (VLSI) or ultra-large scale integrated (ULSI) circuit chips. The term "VLSI" is generally associated with chips containing thousands or millions of metal oxide semiconductor field effect transistors (MOSFETs). The term "ULSI" is generally associated with chips containing billions, or more, MOSFETs. We'll avoid the use of these descriptive terms in this book and focus simply on "digital and analog CMOS circuit design." We'll also introduce circuit simulation using SPICE (simulation program with integrated circuit emphasis). The introduction will be used to review basic circuit analysis and to provide a quick reference for SPICE syntax. CMOS circuit design (the idea and basic concepts) was invented in 1963 by Frank Wanlass while at Fairchild Semiconductor; see US Patent 3,356,858, [5]. The idea that a circuit could be made with discrete complementary MOS devices, an NMOS (n-channel MOSFET) transistor (Fig. 1.6) and a PMOS (p-channel) transistor (Fig. 1.7) was quite novel at
the time given the immaturity of MOS technology and the rising popularity of the bipolar junction transistor (BJT) as a replacement for the vacuum tube. In 1968 a group led by Albert Medwin at RCA made the first commercial CMOS integrated circuits (the 4000 series of CMOS logic gates). At first CMOS circuits were a low-power, but slower, alternative to BJT logic circuits using TTL (transistor-transistor logic) digital logic. During the 1970s, the makers of watches used CMOS technology because of the importance of long battery life. Also during this period, MOS technology was used for computing processor development, which ultimately led to the creation of the personal computer market in the 1980s and the use of internet, or web, technology in the 1990s. It’s likely that the MOS transistor is the most manufactured device in the

4.2. SR Latch Circuit (using NAND gates)-
a SR latch using two NAND2 gates. Note in order to hold (preserve) a state, both of the external trigger inputs must be equal to logic “1”. The state of the circuit can be changed by pulling the set input or reset input to zero.

Figure 1. CMOS SR latch circuit based on NAND2 gates

Figure 2. Simplified schematic and timing diagram latch.
The gate level schematic and the corresponding block diagram representation of the NAND-based SR latch. Note that a NAND-based SR latch responds to an active low input signals, while the NOR-based SR latch responds to an active high inputs. The small circles at the S and R input terminals indicate that the circuit responds to active low input signals. The truth table of the NAND SR latch is also shown in Fig. 5.8. The same approach used in the timing analysis of the NOR-based SR latches can be applied to NAND-based SR latches.

3. CMOS D-LATCH-: As an example, consider the simple D-latch circuit shown in Fig. 3.20. The gate level representation of the D-latch is simply obtained by modifying the clocked NOR-based SR latch circuit. It can be seen from Fig. 3.20 that the output Q assumes the value of the input D when the clock is active (i.e. for CK=“1”). When the clock signal goes to zero, the output will simply preserve its state. Thus, the CK input acts as an enable signal which allows data to be accepted into the D-latch. The transistor implementation of a D-latch circuit can be realized as shown in Fig. 3.21. Fig 3.21 shows a basic two-inverter loop and two CMOS transmission gate (TG) switches. The CMOS transmission gate (TG) consists of one nMOS and one pMOS transistor connected in parallel and acts as a bidirectional switch between nodes A and B which is controlled by signal C, as illustrated.

Figure 3. CMOS implementation of the D-latch

Figure 4. Simplified schematic and timing diagram, showing the setup and hold times.

Note that the valid D input must be stable for a short time before (setup time, $t_{\text{setup}}$) and after (hold time, $t_{\text{hold}}$) the negative clock transition, during which the input switches open and the loop switch, closes. Note that any violation of the setup and hold times can cause metastability problems which can lead to unpredictable transient behaviour. Fig. 5.25 shows the two-stage master-slave flip-flop circuit constructed by two D-latch circuits. The first stage (master) is driven by the clock signal, while the second stage (slave) is driven by the inverted clock signal. Thus the master stage is a positive level-sensitive, while the slave stage is negative.

4. SRAM-

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power
consumption. Technology scaling results in a significant increase in leakage current of CMOS devices. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design. As the integration density of transistors increases, power consumtion has become a major concern in today’s processors and SoC designs. Considerable attention has been paid to the design of low power and high performance SRAMs as they are critical components in both handheld devices and high performance processors. Different design remedies can be undertaken; a decrease in supply voltage reduces quadratic ally the dynamic power and reduces leakage power linearly to the first order. A six transistors (6T) SRAM cell configuration is proposed in this paper which will be a solution to the encountered problems in deep submicron and nano scale. The objective of this paper is to investigate the transistor sizing of the 6T SRAM cell for optimum power and delay. A bitline balancing scheme and transmission gate scheme are proposed for high performance operation of SRAM cell. Cadence simulation results confirm that the proposed scheme achieves nearly 40% of power savings compared to other.

5. DRAM (Dynamic Random Access Memory)

Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid operations on a memory device are reading the data stored in the device, writing (or storing) data in the device, and refreshing the data periodically. To improve efficiency and speed, a number of methods for reading and writing the memory have been developed.
Layouts are drawn and simultaneous comparisons are carried out using Electric CAD tool and basic simulations were carried out with LT Spice

6. REFERENCES-


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