Space Vector Modulation for Power Smoothing in Wind Generation
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Abstract:
This paper presents a capacitor-clamped three-level inverter-based supercapacitor direct integration scheme for wind energy conversion systems. The idea is to increase the capacitance of clamping capacitors with the use of supercapacitors and allow their voltage to vary within a defined range. Even though this unique approach eliminates the need of interfacing dc–dc converters for supercapacitors, the variable voltage operation brings about several challenges. The uneven distribution of space vectors is the major modulation challenge. A space vector modulation method is in this paper to address this issue and to generate undistorted currents even in the presence of dynamic changes in supercapacitor voltages. A supercapacitor voltage equalization algorithm is also presented. Moreover, control strategies of the system are discussed in detail. Simulation results are presented to verify the efficacy of the system in suppressing short-term wind power fluctuations.

Keywords: Capacitor-clamped three-level inverter, space vector modulation (SVM), supercapacitor energy storage, wind energy.

I. INTRODUCTION

Short-term power exchange using supercapacitors is actively pursued in wind power generation schemes as evident from the large number of techniques reported in the literature [1]–[9]. These techniques can be divided into three major categories depending on the way the supercapacitors are connected to the wind power system. In the first category, supercapacitors are connected to the dc link of the back-to-back converter system. Even though the direct connection to the dc link is the simplest, it suffers from drawbacks such as limited voltage range and limited control over the power flow. Effects of these issues can be somewhat reduced if an intermediate dc–dc converter is placed between the supercapacitor and the dc link. This dc–dc converter needs to possess the bidirectional power flow capability, and therefore, at least two fast switching devices rated to the peak power are required. The addition of such devices gives rise to increased switching and conduction power losses. They also can cause stability issues, particularly at high inrush currents. Furthermore, interfacing converters add cost and weight to the system, mainly with their large inductors rated for the peak power transfer [10].

A three level bidirectional dc–dc converter has been to reduce voltage stresses on switching devices and to reduce the filter inductance. However, it needs four switches and a flying capacitor. Therefore, the interfacing dc–dc converter appears to have increased power losses, system cost, and complexity, even if an optimized design is used. The second category uses the common ac bus for power exchange, and it requires an additional dc–dc converter, a dc–ac inverter, and a coupling transformer. This topology has the capability of acting as a static synchronous compensator as well for voltage support at the point of common coupling of the grid. However, aforementioned drawbacks are common for this configuration as well but could be alleviated if a direct integration scheme with full controllability is available. The third category is based on this idea, and it uses a dual-inverter structure for direct integration of supercapacitors. Even though this arrangement eliminates interfacing dc–dc converters, it needs two inverters and a coupling transformer with open ends in the inverter side. This variable voltage operation gives rise to three major problems. Unequal blocking voltages and increased voltage slew rates (dv/dt) experienced by some switching devices as a result of unbalanced voltages are the first issue. Large band gap devices such as SiC, GaN, and thin-film diamond devices are expected to break the 6.5-kV limit of blocking voltage in traditional Si devices. Therefore, in the long run, this would not be a significant problem in implementing the system in medium-voltage wind energy conversion systems. The second problem is the unequal distribution of instantaneous power losses among switching devices. As a result, some devices tend to get heated more than the others. Heat sinks should be overrated to protect switching devices from these thermal stresses. The design process of heat sinks in such situations is an area that demands detailed analysis and is presently being investigated.

Table 1

<table>
<thead>
<tr>
<th>Switching state (S)</th>
<th>Gate signals (GCD, GMD)</th>
<th>Vg</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0011</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0101</td>
<td>Vg</td>
</tr>
<tr>
<td>2</td>
<td>1000</td>
<td>Vg - Vdc</td>
</tr>
<tr>
<td>3</td>
<td>1100</td>
<td>Vg</td>
</tr>
</tbody>
</table>

The third problem is the uneven distribution of space vectors. A detailed analysis of this issue is given in Section II. To tackle this issue and produce undistorted currents even in the presence of dynamic changes in supercapacitor voltages, a
space vector modulation method has been developed and is presented in Section III. In order to achieve supercapacitor voltage equalization, a small vector selection-based controller is in Section IV which controls the supercapacitor charging/discharging process accordingly. Another key concern of the direct connection approach is the exposure of supercapacitors to high-frequency switching current spikes. In fact, at high frequencies, supercapacitors behave as resistors, and thus, expected capacitive effect is no longer available. Therefore, the system requires three electrolytic capacitors to support supercapacitors at high frequencies. A discussion on supercapacitor sizing is presented in Section V. Control strategies of the system are discussed in detail in Section VI. Simulation and results are presented in Sections VII and VIII, respectively, to verify the efficacy of the system in suppressing short term wind power fluctuations.

II. EFFECTS OF CAPACITOR VOLTAGE VARIATIONS

The terminal voltage of a supercapacitor varies with its stored energy. Moreover, 50% reduction of supercapacitor voltage from the maximum value yields 75% discharge of the stored energy. Therefore, in order to ensure maximum utilization of supercapacitors, they are allowed to operate at variable voltages, ranging from 400 to 800 V for example. As mentioned in the introduction, this variable voltage operation creates three major problems. The purpose of this section is to present an analysis on the third problem, i.e., the uneven distribution of space vectors. The first step of this analysis is the definition of possible voltage levels in a capacitor-clamped three-level inverter. The line to-ground voltage of each leg of the inverter can have maximum of four voltage levels. These four voltage levels, corresponding gate signals, and switching states for the leg “a” of the inverter are given in Table I. The other two legs also follow the same pattern. If supercapacitor voltages are balanced, the second and third voltage levels (V_{dc} and V_{dc}-V_{sc}) become equal, and hence, the total number of discrete voltage levels get reduced to three (0, V_{dc}/2, and V_{dc}). In this particular situation, the switching states “1” and “2” produce the same line-to-ground voltage, i.e., v_{ag}=V_{dc}/2. Therefore, these two states are called redundant states. Under this balanced condition, the system acts as a three-level inverter. The corresponding space vector distribution is shown in Fig. 2(a). Equations (1) and (2) are used together with Table I in calculating the coordinates of these vectors. Theoretically, for a converter with n number of voltage levels per leg, there will be n^2 number of total space vectors. Accordingly, this three-level inverter has a total of 3^3 (27) vectors. However, due to overlapping, only 19 discrete vectors are visible in Fig. 2(a).

If supercapacitor voltages are reduced to one-third of the dc link voltage, each leg of the inverter can produce four different voltage levels (0, V_{dc}/3, 2V_{dc}/3, and V_{dc}). Therefore, in this case, the same system operates as a four-level inverter with the space vector distribution shown in Fig. 2(b). In order to differentiate each and every vector point without being overlapped, slight changes have been introduced to supercapacitor voltages. Out of 64 possible vectors, 63 are visible in this diagram. The missing one is located at the origin. However, if supercapacitor voltages are equal, overlapping occurs, and hence, out of 64, only 37 vectors appear in the space vector diagram. Similarly, if supercapacitor voltages are increased to two-thirds of the dc-link voltage, each leg of the inverter again produces four different voltage levels (0, V_{dc}/3, 2V_{dc}/3, and V_{dc}). Therefore, the system operates as a four-level inverter in this case too with the space vector distribution shown in Fig. 2(c). Even though this diagram looks very similar to Fig. 2(b), positions of some vectors are interchanged.

In the system, the lower limit for supercapacitor voltages is kept at V_{dc}/3. The space vector diagram shown in Fig. 2(b) corresponds to this situation. Similarly, supercapacitor voltages are upper bounded to 2V_{dc}/3. The corresponding space vector distribution is shown in Fig. 2(c). As supercapacitor voltages are increased from the lower limit, the innermost hexagon, shown in Fig. 2(b), expands, while the other inner hexagons shrink. When supercapacitor voltages reach V_{dc}/2, both inner hexagons get overlapped as shown in Fig. 2(a). Further increase of supercapacitor voltage would cause expansion and shrinkage of inner hexagons which eventually end up as in Fig. 2(c).

![Space vector distribution](image)

Fig. 2. Space vector distribution at different supercapacitor voltage conditions

(a) V_{sc}=V_{sh}=V_{sc}=V_{dc}/3, (b) V_{sc}=0.33V_{dc}, V_{sh}=0.31V_{dc}, and V_{sc}=0.35V_{dc}/3, (c) V_{sc}=0.66V_{dc}, V_{sh}=0.64V_{dc}, and V_{sc}=0.68V_{dc}.

![Simplified block diagram](image)

Fig. 3. Simplified block diagram of the SVM technique.

III. MODULATION STRATEGY

As mentioned in previous sections, imbalanced and unequal capacitor voltages are unavoidable in the system. Operation of flying-capacitor converters at nontraditional voltage ratios has been previously discussed in. They use low-capacity (compared to supercapacitors) electrolytic capacitors, and therefore, voltage balancing and regulation are possible within a short period of time with the use of advanced balancing techniques. However, due to the high capacity, supercapacitors used in the system take long time to change their voltages, and therefore, unequal and unbalanced capacitor voltage conditions can remain for a long time.

The aforementioned modulation strategies are not suitable for this scenario, and therefore, this paper presents a suitable SVM technique which can produce undistorted currents even under unbalanced and unequal voltage conditions. A
simplified block diagram of the SVM technique is illustrated in Fig. 3. The amplitude and the angle θ of the reference voltage vector are calculated using (3) and (4). The currently serving sector of the space vector diagram is derived from the phase angle based on the selection criterion given in Table III.

\[
r = \sqrt{v_d^2 + v_q^2} \\
θ = \tan^{-1}\left(\frac{v_q}{v_d}\right) + θ_{grid}
\]

Where \(v_d^*\) and \(v_q^*\) are d–q-axis components of the reference voltage vector, \(θ_{grid}\) is the angle of grid voltage vector.

After finding the sector, the next step is to find a triangle with three near vectors. The modulation strategy is limited to the use of vectors in two hexagons at a time, i.e., vectors in one of the inner hexagon and the outer hexagon. Therefore, the number of candidate triangles for a given reference vector is limited to four. Selection of the proper triangle is a function of the power management and supercapacitor voltage balancing controllers which will be discussed in Section IV. However, due to the presence of four candidate triangles, eight limit angles, \(θ_1, ..., θ_8\), need to be calculated for a given sector. However, out of these eight angles, only four have to be calculated exclusively. The other four angles can be derived from the calculated angles.

First two limit angles \(θ_1\) and \(θ_2\) are related to the triangles formed with lower small 1 and upper small 2 vectors as shown in Fig. 4(a), whereas the other two limit angles \(θ_5\) and \(θ_6\) are associated with the triangles formed with lower small 2 and upper small 1 vectors as shown in Fig. 4(b). For the simplicity of subsequent calculations, \(x\) and \(y\) are transformed into two variables \(x\) and \(y\) using (5). These two values are directly related to the sides of triangles as marked in Fig. 4. Limit angles are calculated using (6)–(10) where \(α\) is an intermediate variable.

\[
x = \frac{2}{3}(V_a - V_c) \\
y = \frac{2}{3}V_c \\
α = \sin^{-1}\left(\frac{2\sqrt{3}y}{2\sqrt{(x+y)^2 - 3xy}}\right)
\]

The limit angles given in (7)–(10) are valid only for the lower medium vector “310.” The corresponding limit angles for the other medium vector “320” can be derived from these values with the help of (11)–(14). All these limit angles are valid only for the sector 1. Limit angles for other sectors can be derived from these angles with the help of Table IV. Once the limit angles are calculated, the triangle and corresponding three vectors can easily be derived.

After finding the three vectors, the next step is to determine switching times. According to the well-known volt–second balancing principle, a given reference vector can be synthesized using three adjacent vectors.

\[
\theta_1 = α - \sin^{-1}\left(\frac{\sqrt{3}y^2}{2\sqrt{(x+y)^2 - 3xy}}\right)
\]

\[
\theta_2 = \sin^{-1}\left(\frac{\sqrt{3}y^2}{2x}\right)
\]

\[
θ_3 = \pi - \sin^{-1}\left(\frac{\sqrt{3}x}{2y}\right)
\]

\[
θ_4 = \alpha - \pi - \sin^{-1}\left(\frac{y}{\sin(α - 2\pi/3)}\right)
\]

\[
θ_5 = \frac{π}{3} - θ_1
\]

\[
θ_6 = \frac{π}{3} - θ_2
\]

\[
θ_7 = \frac{2π}{3} - θ_3
\]

\[
θ_8 = \frac{π}{3} - θ_4.
\]

The supercapacitor voltage equalization method is based on redundant state selection. Overlapping small vectors, shown in Fig. 2, provide these redundancies. For example, small vectors (100, 322) and (200, 311), shown in Fig. 4, are redundant vector pairs attached to the sector 1. Similarly, there are ten more redundant vector pairs attached to the other five sectors. Half of these redundant vector pairs contribute to supercapacitor charging, while the other half tend to discharge supercapacitors. In other words, vectors on the middle hexagon, shown in Fig. 4, discharge supercapacitors, while the
vectors on the innermost hexagon charge supercapacitors. In order to explain this phenomenon in detail, four equivalent circuits, corresponding to the aforementioned two vector pairs, are shown in Fig. 6. By looking at the current direction of the a-phase in Fig. 6(a), it can be deduced that the supercapacitor attached to leg “a” gets discharged at the small vector “100.” Similarly, the small vector “322” discharges the other two supercapacitors. Therefore, with the proper combination of these two small vectors, discharging rates of supercapacitors can be controlled in sector 1.

![Fig. 6: Block diagram of the supercapacitor voltage equalizer.](image)

**Fig. 7.** Block diagram of the supercapacitor voltage equalizer.

<table>
<thead>
<tr>
<th>Sector</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase with priority</td>
<td>a</td>
<td>c</td>
<td>b</td>
<td>a</td>
<td>c</td>
<td>b</td>
</tr>
<tr>
<td>Most discharged super capacitor</td>
<td>Csa</td>
<td>200</td>
<td>220</td>
<td>020</td>
<td>133</td>
<td>113</td>
</tr>
<tr>
<td>Discharge</td>
<td>100</td>
<td>110</td>
<td>232</td>
<td>233</td>
<td>223</td>
<td>101</td>
</tr>
<tr>
<td>Csb</td>
<td>311</td>
<td>220</td>
<td>020</td>
<td>122</td>
<td>113</td>
<td>313</td>
</tr>
<tr>
<td>Discharge</td>
<td>322</td>
<td>332</td>
<td>020</td>
<td>011</td>
<td>223</td>
<td>323</td>
</tr>
<tr>
<td>Csc</td>
<td>311</td>
<td>331</td>
<td>131</td>
<td>022</td>
<td>002</td>
<td>302</td>
</tr>
<tr>
<td>Discharge</td>
<td>322</td>
<td>332</td>
<td>232</td>
<td>011</td>
<td>001</td>
<td>101</td>
</tr>
</tbody>
</table>

The equivalent circuit in Fig. 6(c) corresponds to the small vector “200” which is on the innermost hexagon shown in Fig. 4. This vector charges the supercapacitor attached to the leg “a” of the converter. Moreover, the other vector of the pair, i.e., “311,” charges the other two supercapacitors as shown in Fig. 6(d). This indicates that the increased use of the small vector “200” charges the supercapacitor Csa at a higher rate than that of the other two. The opposite of this happens if the vector “311” is used. The supercapacitor voltage equalization method is based on this methodology. The corresponding controller block diagram and the lookup table are shown in Fig. 7 and Table V, respectively.

Voltage equalizer, shown in Fig. 7, measures supercapacitor voltages at every switching cycle and sorts them in the ascending order. The output of the minimum–maximum sorting block indicates the supercapacitor which has the highest deviation compared to the voltages of the other two supercapacitors. In the case of a charging condition where all the supercapacitors are supposed to absorb power, the minimum–maximum sorter selects the supercapacitor with lowest voltage as the most deviated one. Table V is used to select suitable small vector for the current sector which, in turn, increases the charging rate of the supercapacitor Csc.

Similarly, if the system operates in the discharging mode and the supercapacitor Cscb, attached to the leg “b” of the converter, shows the highest voltage, it will be discharged at a higher rate compared to the other two. This is done by selecting the supercapacitor Cscb as the most deviated one. At this instance, small vectors are picked up from the discharging row under Cscb in Table V. Voltage equalizer, shown in Fig. 7, measures supercapacitor voltages at every switching cycle and sorts them in the ascending order.

V. SUPERCAPACITORSIZING

Proper sizing of supercapacitors is extremely important for the effective and safe operation of the system. The required capacity of the supercapacitor energy storage system varies with the magnitude and duration of wind power fluctuations which it is supposed to absorb. Power fluctuations caused by the aforementioned wind speed variation have to be compensated by the energy storage system. The supercapacitor model used in simulations is shown in Fig. 8.

![Fig. 8. Supercapacitor model.](image)

**Fig. 8.** Supercapacitor model.

VI. CONTROL STRATEGY

The supercapacitor direct integration scheme is tested on a permanent-magnet synchronous generator-based wind energy conversion system. The corresponding controller block diagram is shown in Fig. 9 which consists of a generator side converter controller and a grid-side inverter controller. The generator torque Tm is derived from the wind turbine model. Moreover, the speed reference for the generator is derived from the wind speed based on the optimal tip speed ratio of the wind turbine.

![Fig. 9. Controller block diagram of the inverter system.](image)

**Fig. 9.** Controller block diagram of the inverter system.

<table>
<thead>
<tr>
<th>TABLE VI</th>
<th>SYSTEM PARAMETERS OF THE SIMULATION SETUP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental frequency</td>
<td>f = 50Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>f_s = 10kHz</td>
</tr>
<tr>
<td>Phase resistance of the generator</td>
<td>R_s = 0.2Ω</td>
</tr>
<tr>
<td>Phase inductance of the generator</td>
<td>L_s = 1mH</td>
</tr>
<tr>
<td>Rated power of the generator</td>
<td>P_m = 100kW</td>
</tr>
<tr>
<td>Capacitance of the dc-link capacitor</td>
<td>C_d = 1mF</td>
</tr>
<tr>
<td>DC-Link voltage</td>
<td>V_d = 1725V</td>
</tr>
<tr>
<td>Capacitance of the supercapacitors</td>
<td>C_s = 60mF</td>
</tr>
<tr>
<td>Inductance of the supercapacitors</td>
<td>L_s = 50mH</td>
</tr>
<tr>
<td>Resistance of the supercapacitors</td>
<td>R_s = 1.9Ω</td>
</tr>
<tr>
<td>Supercapacitor time constant</td>
<td>τ = 1.675s</td>
</tr>
<tr>
<td>Capacitance of the electrolytic capacitor in parallel with the supercapacitor</td>
<td>C_f = 1μF</td>
</tr>
<tr>
<td>Filter resistance of the grid-side inverter</td>
<td>R_f = 0.1Ω</td>
</tr>
<tr>
<td>Filter inductance of the grid-side inverter</td>
<td>L_f = 1mH</td>
</tr>
<tr>
<td>Grid voltage</td>
<td>V_g = 690V</td>
</tr>
<tr>
<td>Cut-in speed of the wind turbine</td>
<td>V_m = 4m/s</td>
</tr>
<tr>
<td>Rated wind speed</td>
<td>V_r = 12m/s</td>
</tr>
<tr>
<td>Flux linkage of the PMSG</td>
<td>φ_m = 0.85V/Φ</td>
</tr>
<tr>
<td>Number of pole pairs in the PMSG</td>
<td>120</td>
</tr>
</tbody>
</table>

The speed error is passed through a proportional integral (PI) controller which, in turn, generates a reference for the q-axis current component i_q. These current references are then compared with actual currents, and the errors are passed through PI controllers to generate voltage references for the subsequent modulation unit. Similarly, the
grid-side inverter controller is implemented in the synchronous reference frame where the d-axis current component \( i_d \) is varied in order to control the active power transfer to the grid. The q-axis current component \( i_q \) is maintained at zero.

The power reference for the grid-side inverter controller is obtained by passing the instantaneous output power of the generator-side converter through a low-pass filter. If no other means of energy storage is present, the residue of the instantaneous power will be absorbed by the dc-link capacitor which, in turn, changes the dc-link voltage. In the system, supercapacitors attached to the grid-side inverter are used to absorb this residue power and thus regulate the dc-link voltage. This is achieved with the appropriate selection of charging and discharging small vectors

VII. SIMULATION RESULTS

Fig. 10 Simulation model for Turbine and Anti wind up system

Main circuit diagram

VII. CONCLUSION

A capacitor-clamped three-level grid-side inverter-based supercapacitor direct integration scheme has been in this paper for mitigating short-term power fluctuations in wind power systems. In order to get the optimum use of supercapacitors, they should be operated under variable voltage conditions. Increase in the blocking voltage is a concern with this variable voltage operation which can be solved with the use of high voltage switching devices such as SiC. The issue of thermal overrating of heat sink associated with the supercapacitor direct integration scheme needs further analysis. The major modulation challenge of the variable voltage operation is the uneven distribution of space vectors. The effects of this phenomenon are discussed in this paper followed by a proposition of an appropriate SVM method. The modulation method is capable of producing desired outputs even in the presence of unevenly distributed space vectors. A small vector selection-based controller is also to control the supercapacitor charging/discharging process with voltage equalization. Simulation results prove the efficiency of the modulation method and charge/discharge controller.

VIII. REFERENCES


